WHAT IS CLAIMED IS:

1. A structure of stacked integrated circuits, comprising:

a substrate having a first surface formed with signal input terminals, and a second surface formed with signal output terminals;

a lower integrated circuit having a first surface and a second surface, the first surface of the lower integrated circuit being adhered to the first surface of the substrate, the second surface of the lower integrated circuit being formed with a plurality of bonding pads;

a plurality of wirings having first ends and second ends, the first ends being electrically connected to the bonding pads of the lower integrated circuit and the second ends being electrically connected to the signal input terminals of the substrate;

an adhesive layer coated on the second surface of the lower integrated circuit, the adhesive layer including adhesive agent and filling elements; and

an upper integrated circuit stacked above the second surface of the lower integrated circuit with the adhesive layer inserted between the upper and lower integrated circuits, wherein the lower integrated circuit is adhered to the upper integrated circuit by the adhesive agent, and a predetermined gap is formed between the lower and upper integrated circuits by the filling elements.

2. The structure of stacked integrated circuits according to claim 1, wherein the signal output terminals of the substrate are metallic balls arranged in the form of a ball grid array (BGA).

3. The structure of stacked integrated circuits according to claim 1, wherein the plurality of wirings are electrically connected to an edge of the second surface of the lower integrated circuit.

4. The structure of stacked integrated circuits according to claim 3, wherein

the plurality of wirings are electrically connected to the lower integrated circuit by way of wedge bonding.

5. The structure of stacked integrated circuits according to claim 1, wherein the adhesive layer is coated on the central portion of the second surface of the lower integrated circuit.

6. The structure of stacked integrated circuits according to claim 1, wherein the adhesive layer is coated on the periphery of the second surface of the lower integrated circuit.

7. A method for manufacturing a structure of stacked integrated circuits, comprising the steps of:

providing a substrate;

providing a lower integrated circuit on the substrate;

electrically connecting the lower integrated circuit to the substrate via a plurality of wirings;

providing an adhesive layer consisting of adhesive agent and filling elements on the lower integrated circuit; and

stacking an upper integrated circuit above the lower integrated circuit with the adhesive layer inserted between the upper and lower integrated circuits, wherein the lower integrated circuit is adhered to the upper integrated circuit by the adhesive agent, and a predetermined gap is formed between the lower and upper integrated circuits by the filling elements.

8. The method for manufacturing the structure of stacked integrated circuits according to claim 7, wherein the plurality of wirings are electrically connected to an edge of the second surface of the lower integrated circuit.

9. The method for manufacturing the structure of stacked integrated circuits according to claim 7, wherein the plurality of wirings are electrically connected to

the lower integrated circuit by way of wedge bonding.

10. The method for manufacturing the structure of stacked integrated circuits according to claim 7, wherein the adhesive layer is coated on the central portion of the second surface of the lower integrated circuit.

11. The method for manufacturing the structure of stacked integrated circuits according to claim 7, wherein the adhesive layer is coated on the periphery of the second surface of the lower integrated circuit.